common n+ contact forms an ohmic contact, and is used as an entrance window (light sensitive window).

On page 2, line 31 through page 3, line 9, please replace with the following paragraph:

In the back-side illuminated photodiodes, the (p+)-(n) junction array, which is created on the non-light sensitive side of the chip, is generally used only for signal readout and therefore can usually be bonded directly to the readout chip or circuitry without obstructing the light from a scintillator. The opposite side (ohmic side) is typically coupled to the scintillator for light detection. This type of array typically operates only in fully depleted mode, which usually requires reverse bias of more than 70 V for the standard 50 ohm-m resistivity silicon or higher biases for lower resistivity material.

On page 5, line 25 through page 6, line 18, please replace with the following paragraphs:

The above and other features of the present invention may be more fully understood from the following detailed description, taken together with the accompanying drawings, wherein similar reference characters refer to similar elements throughout and in which:

FIG. 1 is a cross-sectional view of a detector array produced from high resistivity n-type Si (top) and back-side view (bottom) in an embodiment according to the present invention;

FIG. 2 is a cross-sectional view of a detector array produced from high resistivity p-type Si (top) and back-side view (bottom) in an embodiment according to the present invention;

FIG. 3 is a top view of the topology of a detector array showing separate grids for changing of the pixel sizes by biasing appropriate grids in an embodiment according to the present invention;

FIG. 4 is a top view illustrating the method for joint biasing

of individual grid arrangements by coupling grids together;

FIG. 5 is a top view illustrating the method for individually biasing the grid arrangements;

FIG. 6 is a cross-sectional view of a detector array coupled directly to scintillators and coupled with readout electronics in an exemplary embodiment according to the present invention; and

FIG. 7 is a cross-sectional view of a detector array coupled to scintillators via a interface that functions as a light guide and coupled with readout electronics in another exemplary embodiment according to the present invention.

On page 7, lines 18-26, please replace with the following paragraph:

The photodetector array construction of the present invention may have significant advantages in the mass production process due to lower operating bias voltages, significantly simplified testing, use of thicker Si wafers (less breakage during processing), and possible very high production yields. Use of thicker wafers opens up additional possibilities of processing 6" (instead of 4") (approximately 15 cm (instead of approximately 10 cm)) or even larger diameter wafers leading to the possibility of further reduction in production costs.

On page 8, lines 21-30, please replace with the following paragraph:

The detector array of the present invention may also be used as a radiation hardened detector for high-energy physics research for detection of particles, x-ray, or gamma rays. The radiation hardness of this structure may be achieved through simplified construction (lack of the field plates and excessive guard rings) and relatively low operating bias voltages. The present invention may also find other broad applications.

On page 10, lines 13-23, please replace with the following paragraph:

Referring now to the drawings and in particular to FIG. 1, a light sensitive array 10 in an embodiment according to the present invention is constructed from n-type silicon (Si) 14. The n-type Si 14 preferably is high resistivity Si, such resistivity preferably being between 10 ohm-m to 200 ohm-m. The light sensitive array 10 has a common p^+ light sensitive contact 20 on the front-side and ohmic contacts implemented as a n^+ pixelated array 24 on the back-side. The n^+ pixels on the back-side preferably are coupled to readout electronics 25 via pre-amplifiers (not shown).

On page 11, line 26 through page 12, line 12, please replace with the following paragraph:

The operational bias voltage, $-V_B$ 34 applied to the p^+ light sensitive contact 20 may be lower by up to a factor of four than the bias voltage necessary to operate standard back-side illuminated silicon structures fabricated from identical starting materials. During testing of the light sensitive array 10, it is not required to measure each of the (thousands of) individual pixels at a great expenditure of time and resources. Instead, a complete evaluation of the array may be achieved with only two measurements. The first measurement is of the leakage current of the fully biased p^+ light sensitive contact 20 (without biasing the p^+ grid 28). The second measurement is of the leakage current of the fully biased p^+ grid 28 (without biasing the p^+ light sensitive contact 20). Measured values of the leakage currents less than 100 $\mu A/m^2$ for the p^+ light sensitive contact 20 and p^+ grid 28 may be an indication of the proper operation of the entire light sensitive array 10. Leakage currents as low as 1 $\mu A/m^2$ may be encountered during these measurements.

On page 13, line 19 through page 14, line 5, please replace with the following paragraph:

The operational bias voltage, $+V_B$ 134 applied to the n^+ light sensitive contact 120 may be lower by up to a factor of four than the bias voltage necessary to operate standard back-side illuminated silicon structures fabricated from identical starting materials. During testing of the light sensitive array 110, it is not required to measure each of the (thousands of) individual pixels at a great expenditure of time and resources. Instead, a complete evaluation of the array may be achieved with only two measurements. The first measurement is of the leakage current of the fully biased n^+ light sensitive contact 120 (without biasing the n^+ grid 128). The second measurement is of the leakage current of the fully biased n^+ grid 128 (without biasing the n^+ light sensitive contact 120). Measured values of the leakage currents less than 100 $\mu A/m^2$ for the n^+ light sensitive contact 120 and n^+ grid 128 may be an indication of the proper operation of the entire light sensitive array 110. Leakage currents as low as 1 $\mu A/m^2$ may be encountered during these measurements.

On page 14, line 6 through page 15, line 27, please delete the paragraphs.

On page 15, line 28 through page 16, line 21, please replace with the following paragraphs:

FIG. 3 shows a construction of a grid pattern where high resistivity n-type Si 14 is used as the starting material. The readout side of a device 50 in this case includes at least two grid patterns. One of the grid patterns 52 surrounds a second (interior) set of grid patterns 54. In this case, it is possible to achieve one pixel size by biasing the exterior sections of the grid 52 using voltage V_1, and to change the size of the pixels by biasing the

interior sections of the grid 54 using voltage V_2. Using this method, the pixel size and the resulting spatial resolution of the detector array may be electronically regulated.

Referring now to FIG. 4, the individual interior grid arrangements 54 may be jointly biased by a single externally applied voltage using V_2 if the individual grids are coupled via a conductive bridge 60 placed over an electrical insulation layer 62 which electrically isolates the interior grid 54 from the exterior grid 52. This may be implemented as a part of planar silicon device fabrication using standard photolithography tools, or after the wafers have been processed on individual detectors using physical masks to define areas for insulator and metal evaporations. Referring now to FIG. 5, the interior grids such as 54 and 56 may be individually biased through external connections to each such grid using voltages V_2 54, V_3 56, and the like.

On page 16, after line 21, please add the following new paragraphs:

The light sensitive array 10 in FIG. 1 of the present invention may be directly coupled to a scintillator. For example, FIG. 6 illustrates a light sensitive array 610, which has substantially identical structure as the light sensitive array 10. An entrance window 620 of the light sensitive array 610 is directly coupled to a scintillator 640, which may be selected from CsI(Tl), $CdWO_4$, NaI(Tl), LSO and BGO scintillators, or any other suitable scintillators.

In addition, the light sensitive array 10 of the present invention may be coupled to a scintillator via an interface that functions as a light guide between its entrance window and the scintillator. For example, FIG. 7 illustrates a light sensitive array 710, which has substantially identical structure as the light sensitive array 10. The light sensitive array 710 is coupled to a scintillator 740 via an interface 742 disposed between its entrance